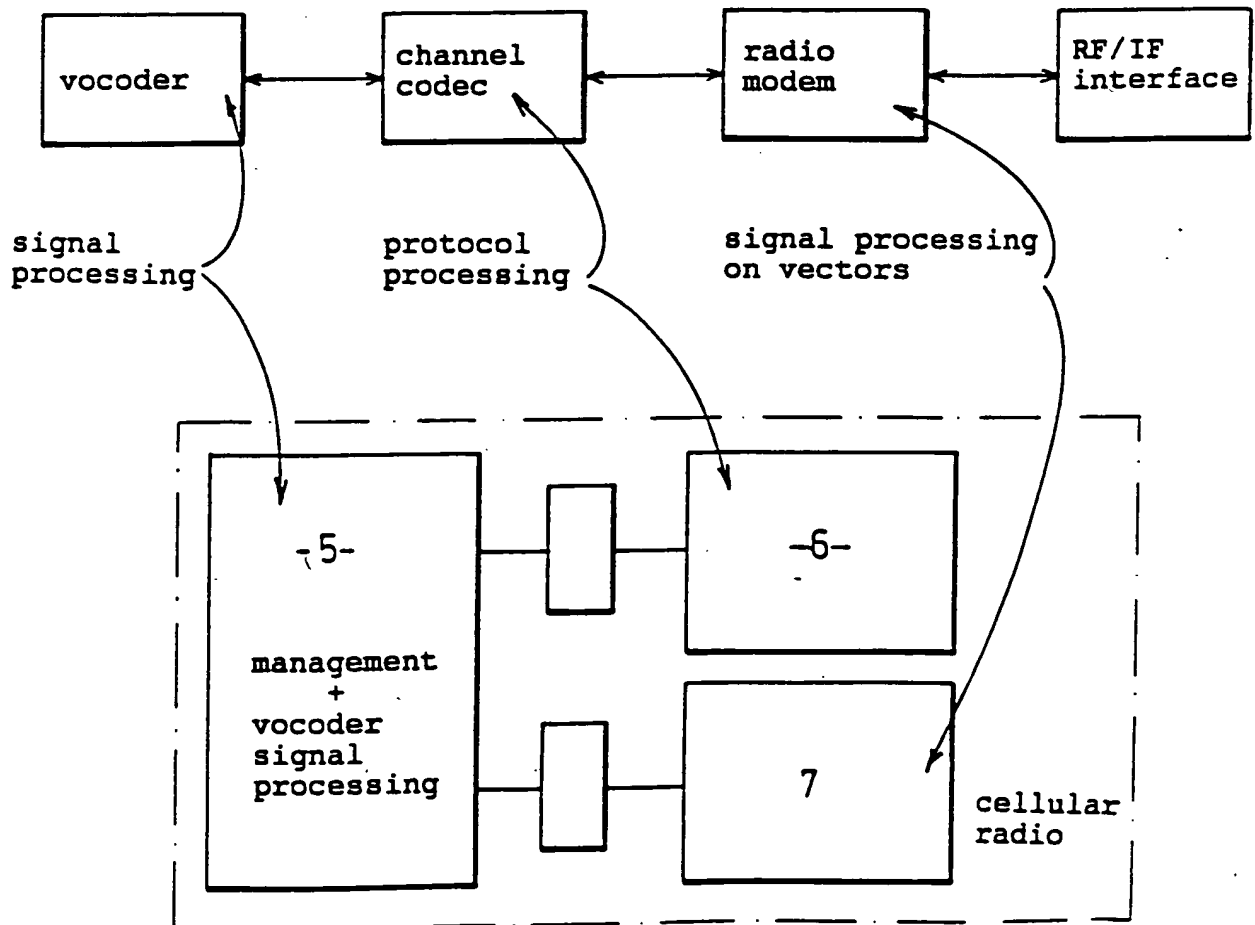
FIG. 1FIG. 2

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PERFORMANCE OF CHANNEL CODEC ROUTINES

routines	DSP utilisation C5x	proc. protocol PP utilisation
16 bit CRC identification	6 instr/ bit 5 instr/ bit	4 instr/ bit 1 instr/ bit.
RATIO		
sel/instr efficiency no. of trans. MIPS	$\times 1$ 58 KTx 28 MIPS	$\times 2.2$ 6.5 KTx $28 \times 2.2 = 62$ MIPS DSP

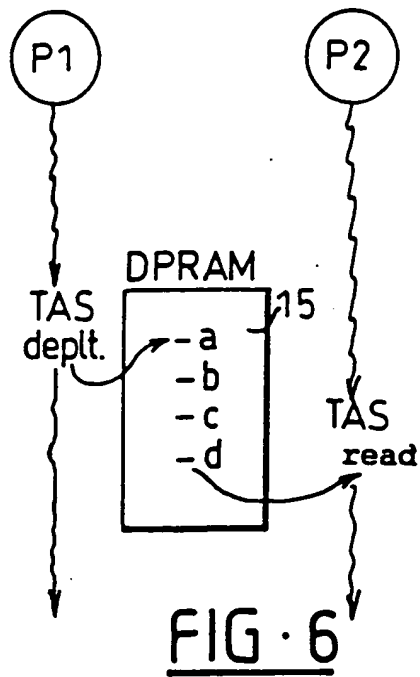
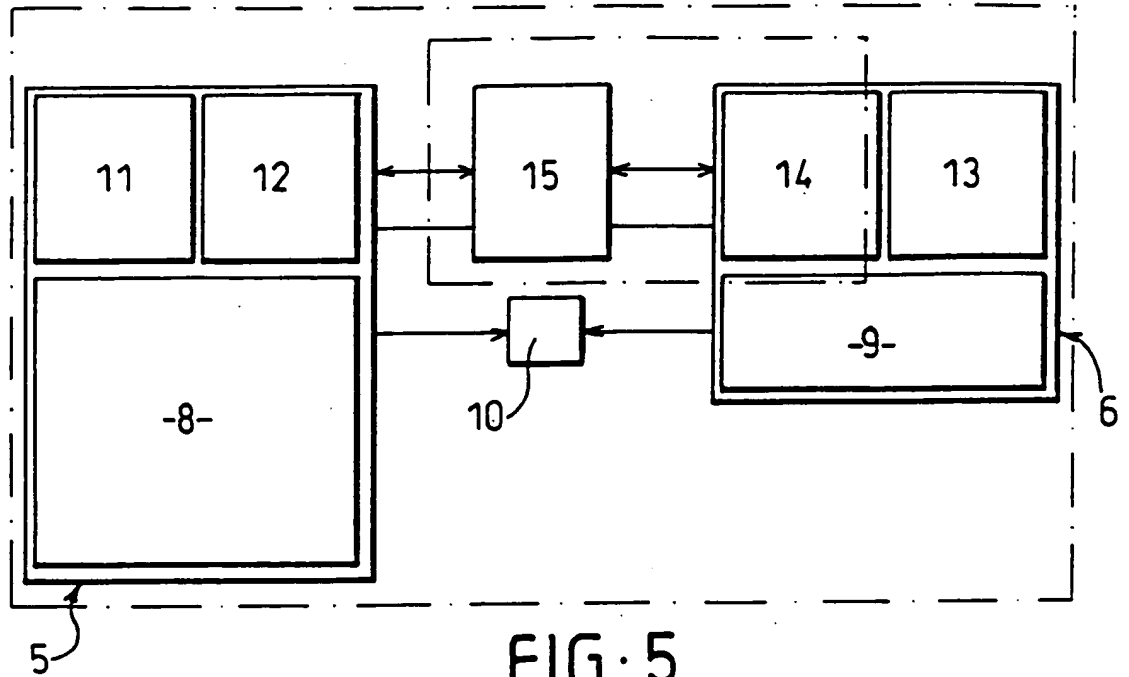
FIG. 3

PERFORMANCE OF MODEM ROUTINES

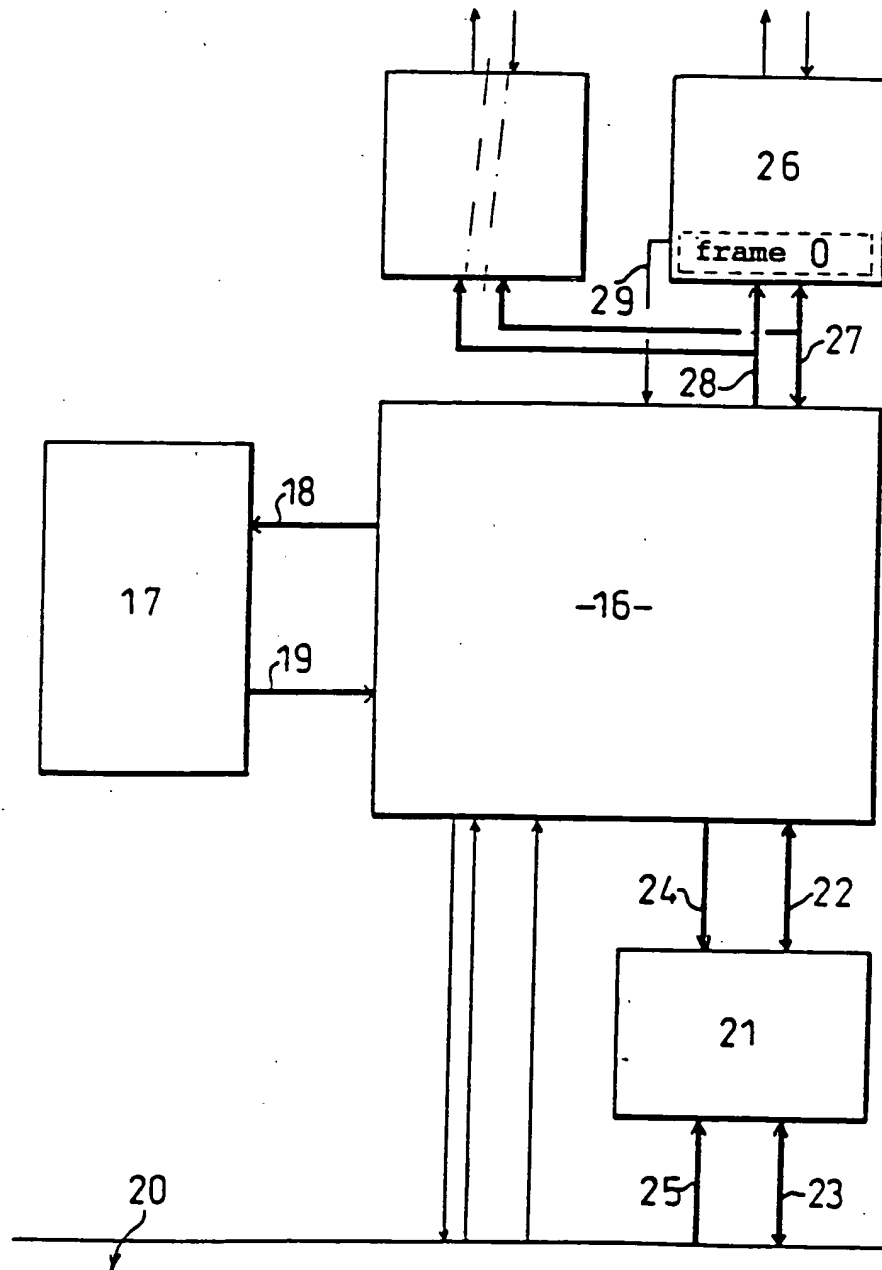
routines	DSP utilisation C5x	array proc.
metric computation 57 symbols (4 samples)	43800 cycles	4400 cycles
RATIO		
instruction setting efficiency MIPS	$\times 1$ 28 MIPS	$\times 10$ $28 \times 10 = 280$ MIPS DSP

FIG. 4

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FIG. 7

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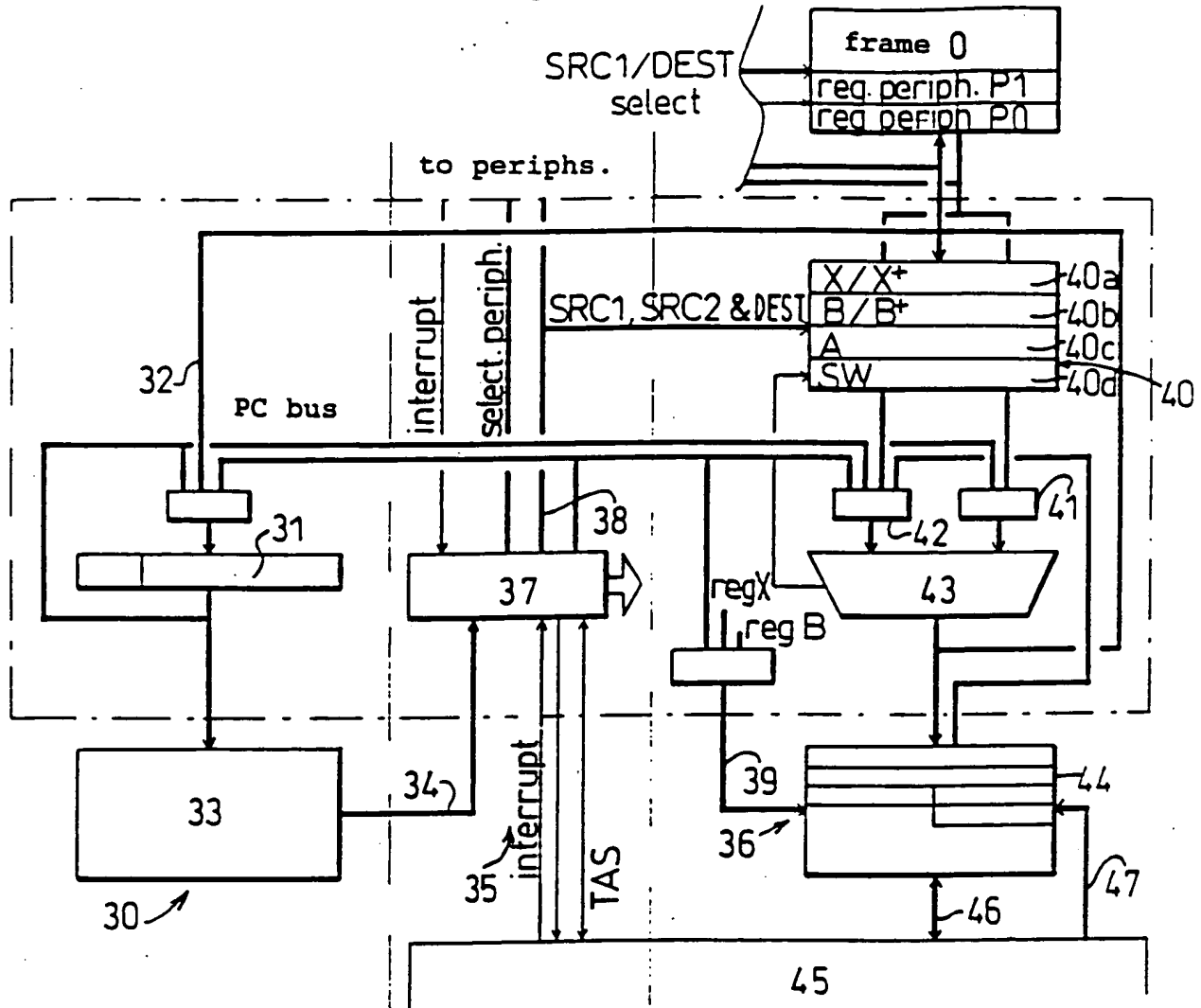


FIG. 8

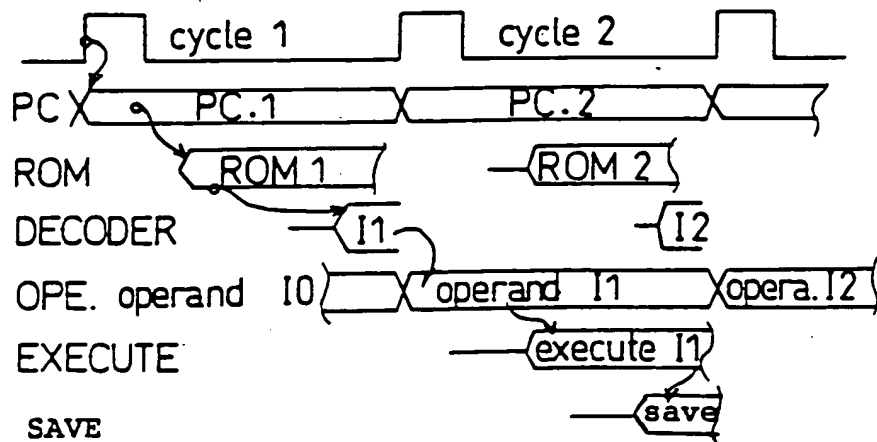


FIG. 9

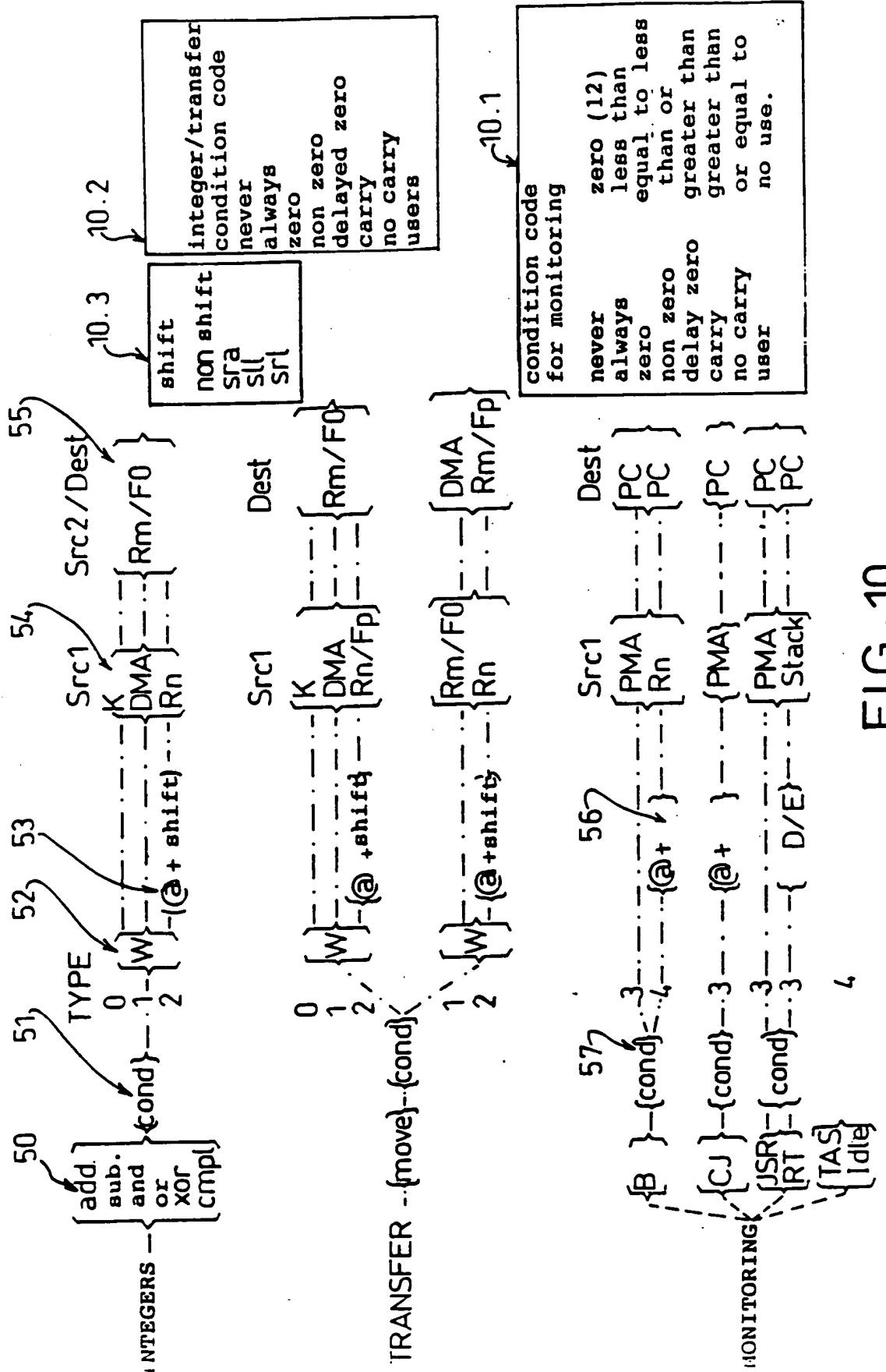
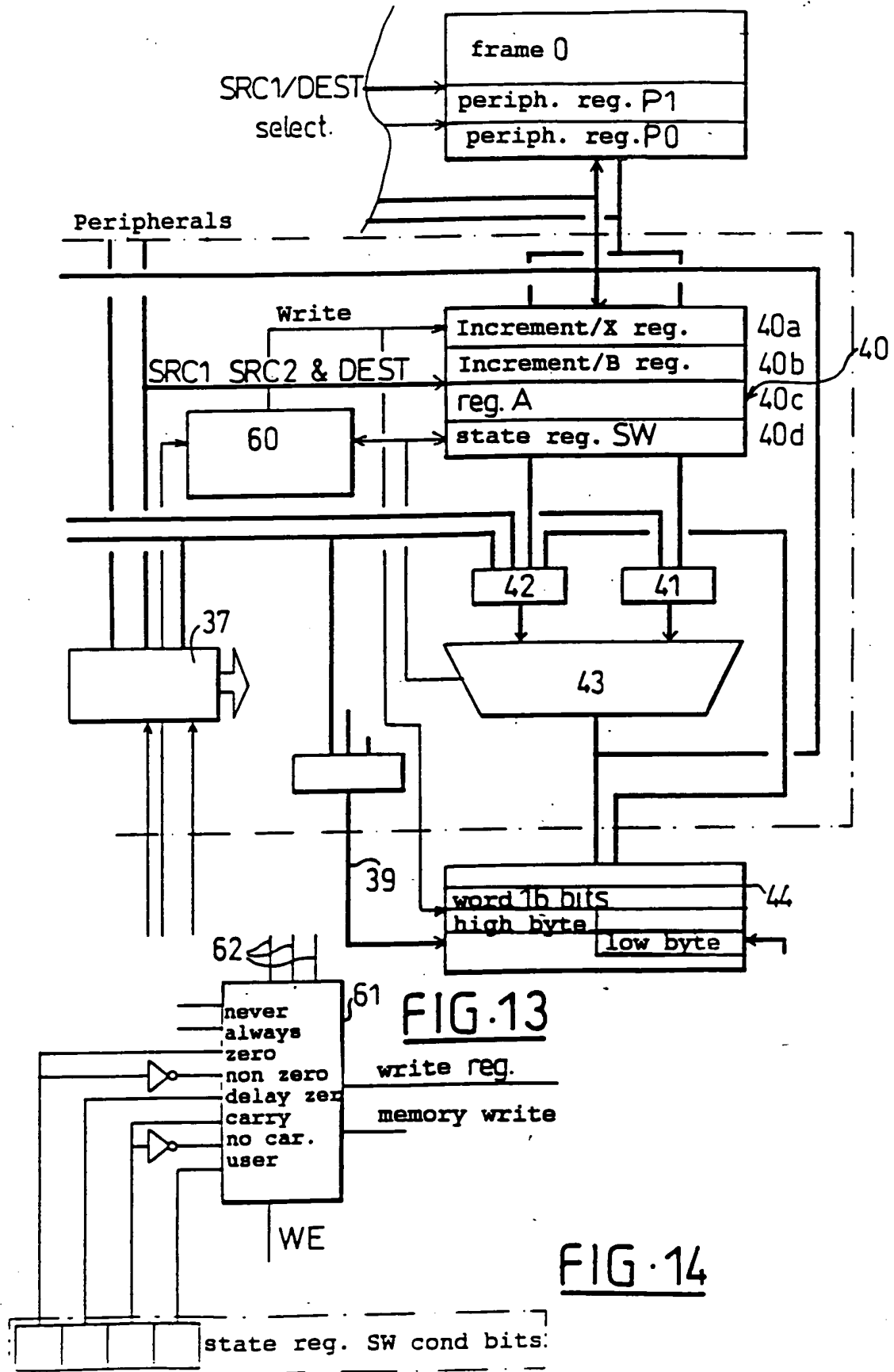


FIG. 10

FIG. 11

FIG. 12



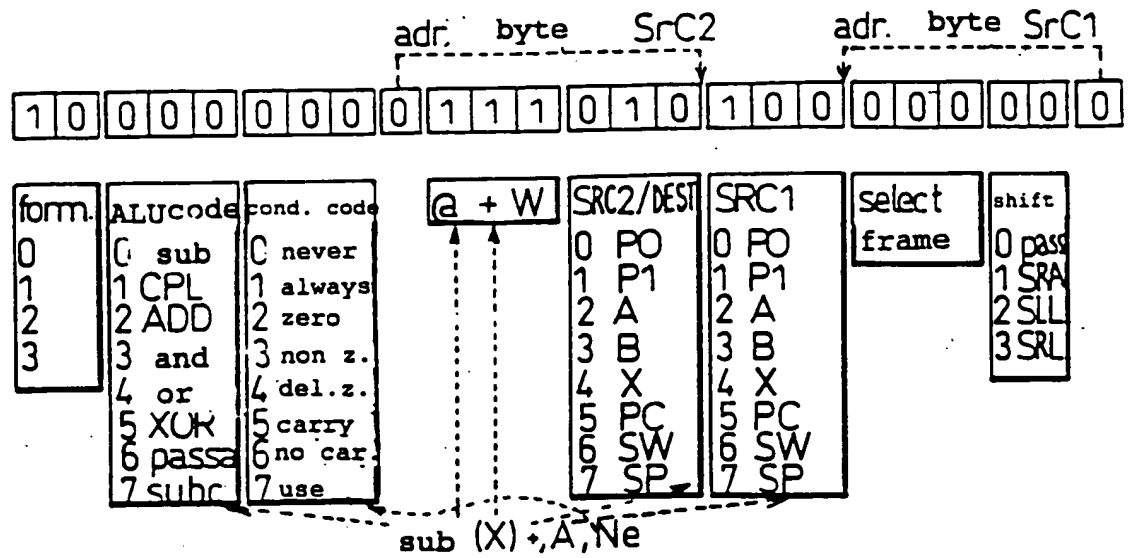


FIG. 15

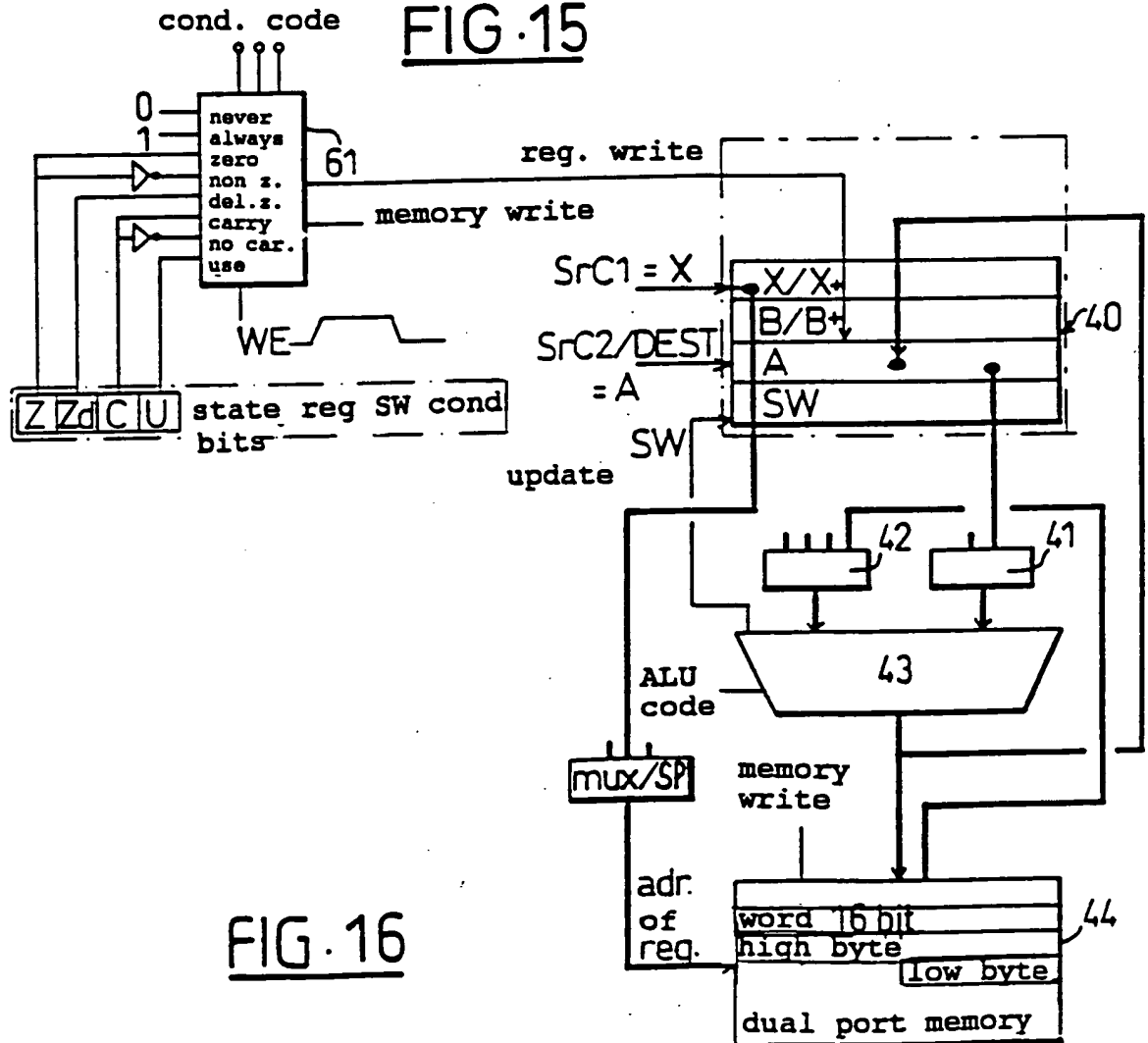


FIG. 16

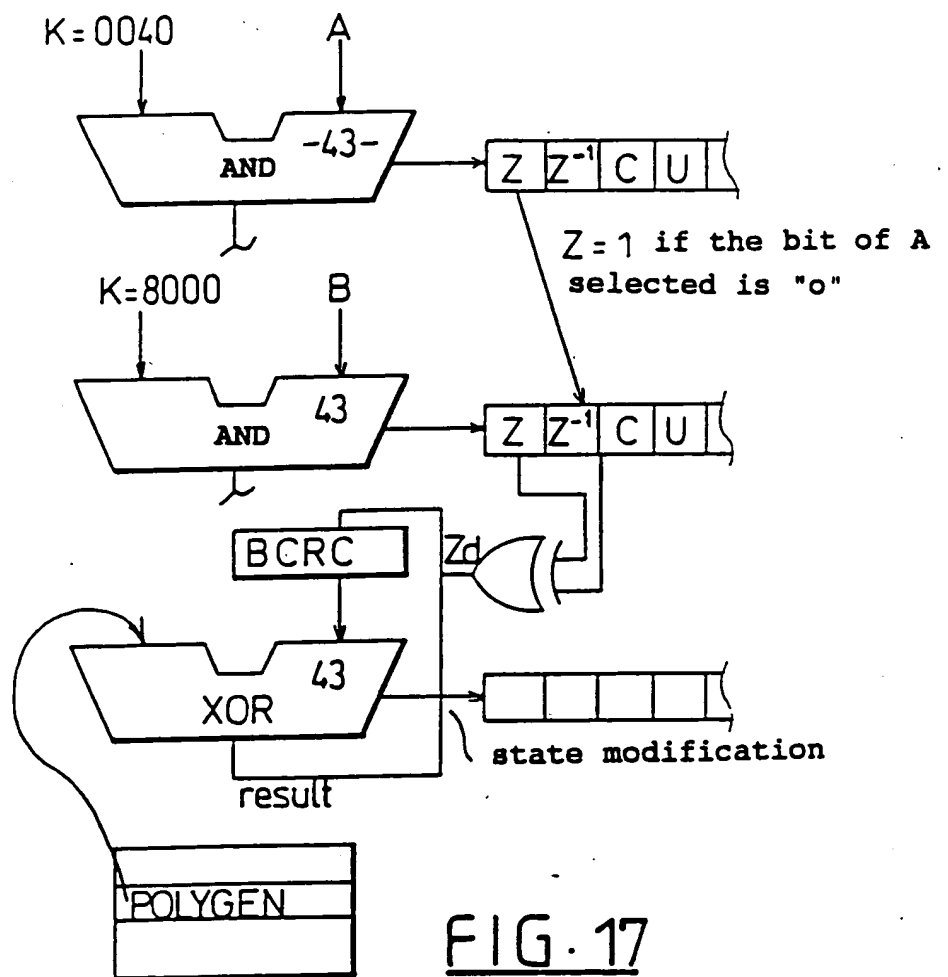


FIG. 17

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